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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,307	02/10/2004	Ching-Nan Hsiao	10113741	1517

34283 7590 03/08/2007

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EXAMINER	
THOMAS, TONIAE M	
ART UNIT	PAPER NUMBER
2822	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/775,307	HSIAO ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/21/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 21 December 2006 has been entered.

2. Currently, claims 1-12 are pending.

Information Disclosure Statement

3. The examiner has considered the information disclosure statement (IDS) submitted on 21 December 2006.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

4. *Claims 1, 9, 10 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Prall et al. (US 2004/0130934 A1).*

The Prall et al. application publication (referred to hereinafter as Prall) discloses a method for fabricating an NROM memory cell (see figs. 1, 2 and accompanying text). The method comprises: providing a semiconductor

substrate having a trench 22 (fig. 1 and par. 0046); forming doped areas 24, 26, acting as bit lines, in the semiconductor substrate near its surface and the bottom of the trench (fig. 1 and par. 0046); forming bit line insulating layers 32, 42, simultaneously by thermal oxidation, over each of the doped areas 24, 26 (fig. 2 and par. 0049, lines 1-5);[1] forming a conformable layer 44 over a sidewall of the trench and the bit line insulating layers to locally store electric charge (fig. 2 and par. 0051, lines 4-10); and forming a conducting layer 38 over the conformable layer and filling in the trench (fig. 2 and par. 0048, lines 7-8).

A gate dielectric layer, thin oxide layer 42, is formed between the conformable layer 44 and the trench surface (fig. 2 and par. 0051, lines 1-4).

The conducting layer 38 is a poly layer (par. 0048, lines 7-8).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. *Claims 6, 8 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prall.*

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[1] The insulating layer 32, 42 is formed over the surface of doped areas 24 exposed in the sidewall of the trench 22.

Prall does not teach: that the bit line insulating layers are formed to a thickness of 300 to 2000 Å, that the conformable layer is formed to a thickness of 50 to 110 Å, or that the gate dielectric layer is formed to a thickness of 50 Å. However, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to: form the bit line insulating layers to a thickness of 300 to 2000 Å, and form the conformable layer to a thickness of 50 to 110 Å; since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art (*In re Aller*, 105 USPQ 233). Furthermore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the gate dielectric layer to a thickness of 50 Å, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art (*In re Boesch*, 205 USPQ 215 (CCPA 1980)).

6. *Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prall et al. in view of Hoffman et al. (US 5,998,261).*

As explained above, Prall discloses forming doped areas 24, 26, which act as bit lines. While Prall discloses using ion implantation to form the doped areas (par. 0047, lines 1-9), the application publication does not teach forming the doped areas by: forming a silicon nitride spacer over the sidewall of the trench; performing ion implantation in the substrate using the spacer as a mask; and removing the spacer.

The Hoffman et al. patent (referred to hereinafter as Hoffman) discloses a method for forming a memory device (see figs. 1-5 and accompanying text). The method comprises: forming a silicon nitride spacer 8 over the sidewall of a trench (fig. 3 and col. 3, lines 62-67); performing ion implantation in the substrate, using the spacer as a mask, to form doped regions 14a at the bottom of the trench (fig. 3 and col. 4, lines 2-12); and removing the spacer (fig. 4 and col. 4, lines 18-20). The spacer 8 prevents a shift in the threshold voltage of the vertical MOS transistor subsequently created on the sidewall of the trench (col. 4, lines 10-12).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Prall by using a silicon nitride spacer in the formation of the doped area 26 at the bottom of the trench 22, as taught by Hoffman, since the spacer prevents a shift in the threshold voltage of the vertical MOS transistor subsequently created on the sidewall of the trench (Hoffman - col. 4, lines 10-12).

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Prall in view of Forbes (US 2003/0235076 A1).

While Prall discloses forming a conformable layer 44 to locally store charge, Prall does not teach that the conformable layer is a silicon-rich oxide layer.

Forbes discloses a method for forming a multi-state NROM device. Forbes lists several insulating materials that may be used as a charge storing

or charge trapping layer in multi-state NROM devices (par. 0046, lines 4-15). These materials include silicon nitride and Si-rich oxide (par. 0046, lines 9-10).

The conformable layer 44 disclosed in Prall is a silicon nitride layer; which, as stated above, is used to locally store charge. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use a silicon-rich oxide layer in place of the nitride layer as the conformable layer of Prall, since the conformable layer is a charge-storage layer, and silicon-rich oxide films are charge storage films that can be used for storing charge in multi-state memory cell devices.

8. *Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Prall and in view of Hoffman as applied to claim 2 above, and further in view of Savant et al. (Electronic Circuit Design An Engineering Approach).*

Prall discloses that doped areas 24, 26 are n^+ regions formed by ion implantation (par. 0047, lines 1-9). However, Prall does not disclose that ions implanted to form the doped areas are phosphorous ions.

Savant et al. (referred to hereinafter as Savant) teaches that phosphorus is one impurity used to form n-type silicon (see Appendix B: Principles of Semiconductor Physics, under section B.2 Impurities in Semiconductors, and subsection B.2.1 n-type Semiconductor, page A-40).

Absent evidence to the contrary, the semiconductor substrate 20 of Prall is a silicon substrate. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the doped areas of Prall by

art, at the time the invention was made, to form the doped areas of Prall by implanting phosphorus ions into the silicon substrate, since phosphorus is an n-type dopant impurity that can be implanted into silicon to form n-type areas, such as doped areas 24, 26.

Response to Arguments

9. Applicant's arguments filed 21 December 2006 have been fully considered but they are not persuasive.

10. In the reply submitted on 21 December 2006, Applicant argues, "none of the cited references teach or suggest a method for fabricating a multi-bit vertical memory cell including a step of simultaneously forming bit line insulating layers by thermal oxidation over each of the doped areas, as recited in claim 1." Applicant further contends, "in Prall, the alleged 'bit line insulating layers' 32 and 42 are formed in subsequent steps by oxidation over the alleged 'doped areas' 26 at the bottom of the trench ... the alleged 'bit line insulating layers' 28, 32, and 42 are formed in sequential steps by different methods over each of the alleged 'doped areas' 24 near the surface and the alleged 'doped areas' 26 at the bottom of the trench," whereas "claim 1 recites a step of forming bit line insulating layers simultaneously by thermal oxidation over each of the doped areas."

11. It is the examiner's position that, claim 1 as presented in the amendment filed on 21 December 2006, reads on the prior art of record. As explained in the rejection of claim 1 set forth above, Prall discloses a step of forming bit line

insulating layers 32, 42, wherein the layers are formed simultaneously by thermal oxidation over each of the doped areas 24, 26 (fig. 2 and par. 0049, lines 1-5). Specifically, insulating layer 42 is formed over doped areas 24; whereas, insulating layer 32 is formed over the surface of doped area 24 exposed in the sidewall of trench 22. In addition, Prall discloses each limitation of claim 1 as presented in the amendment filed on 21 December 2006. Therefore, claim 1 now stands rejected under 35 USC §102(e) as being anticipated by Prall.

12. The amendment filed on 21 December 2006 has overcome the rejection under 35 USC 112, second paragraph, made of record in the final Office action mailed on 21 September 2006. Accordingly, the 112, second paragraph rejection has been withdrawn.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service

Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

T. M. Thomas
Toniae M. Thomas
Art Unit 2822

TMT
03 March 2007